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SHORTENED CR23X CALIBRATION PROCEDURE

1.0 Purpose

1.1 To describe the procedure for performing CR23X calibration.

2.0 Scope

2.1 Applies only to the CR23X Data logger.

3.0 Test Equipment Needed

3.1 Adjustable 12V Power Supply
3.2 Voltmeter (5 ½ Digit)
3.3 Frequency Counter
3.4 Current Monitor

4.0 Calibration Procedures

1-Current drain:
Check quiescent current. The CR23X quiescent current should be less than 2.1 mA at room temperature with the display off (*0 #).

2-Set CPU Clock Compensation:
To keep the processor clock up and running enter the following program.

Scan Interval 1 second

	Ex. Chan	Del w/ex 0.01s	Del after/ex 0.01s	EX mV
P22	1	9999	0	0

**0 (To compile program)*

To see existing freq. coefficient, connect to CR23X with PC208W terminal emulator and type 19287P [Enter]. It will display: ± xx.xxx + .yyyyy. If there is no frequency coefficient programmed you will see -99999 +0.0000. Connect frequency counter to test point C16Q1 on the CR23X CPU/Analog board. If (xx.xxx) is a negative number add it to the frequency measured. If (xx.xxx) is a positive number subtract it from the frequency measured. If the results are 2,457,600 Hz +/- 2 Hz the frequency coefficient is within specification. If frequency coefficient is not within specification or not programmed, program it as follows:

In terminal mode type 19287:1(last three digits of frequency measured)P [Enter].

Example: If frequency measured is 2,457,569 then type 19287:1569P [Enter].

Remove program 22. (Go to program 22 enter #D to delete instruction.)

3-Set the 32.768 kHz time clock:
Connect a frequency counter to test point C15M. Adjust pot C17M to the frequency of 32.768 kHz with a resolution better than plus or minus .01Hz (example of acceptable values include 32768.005 Hz, or a period lower than 30.517569us and higher than 30.5175873us).

4-Instrumentation Amplifier (IA) Offset Voltage:
To trim the IA offset voltage by means of trim pot R24G, set input storage locations *A 01: to 32 and program 24 as follows:

Scan Interval 1 second

	Option	*Loc.*
P24	*2*	*1*

**0 (To compile program)*
Set input location 8: within ± 20 counts of zero.
Delete Program 24. (Go to program 24 and enter #D to delete instruction.)

5-DAC ZERO
Next trim out the DAC and excitation voltage offsets by utilizing an Excitation with Delay (P22) instruction as follows:

Scan Interval 1 second

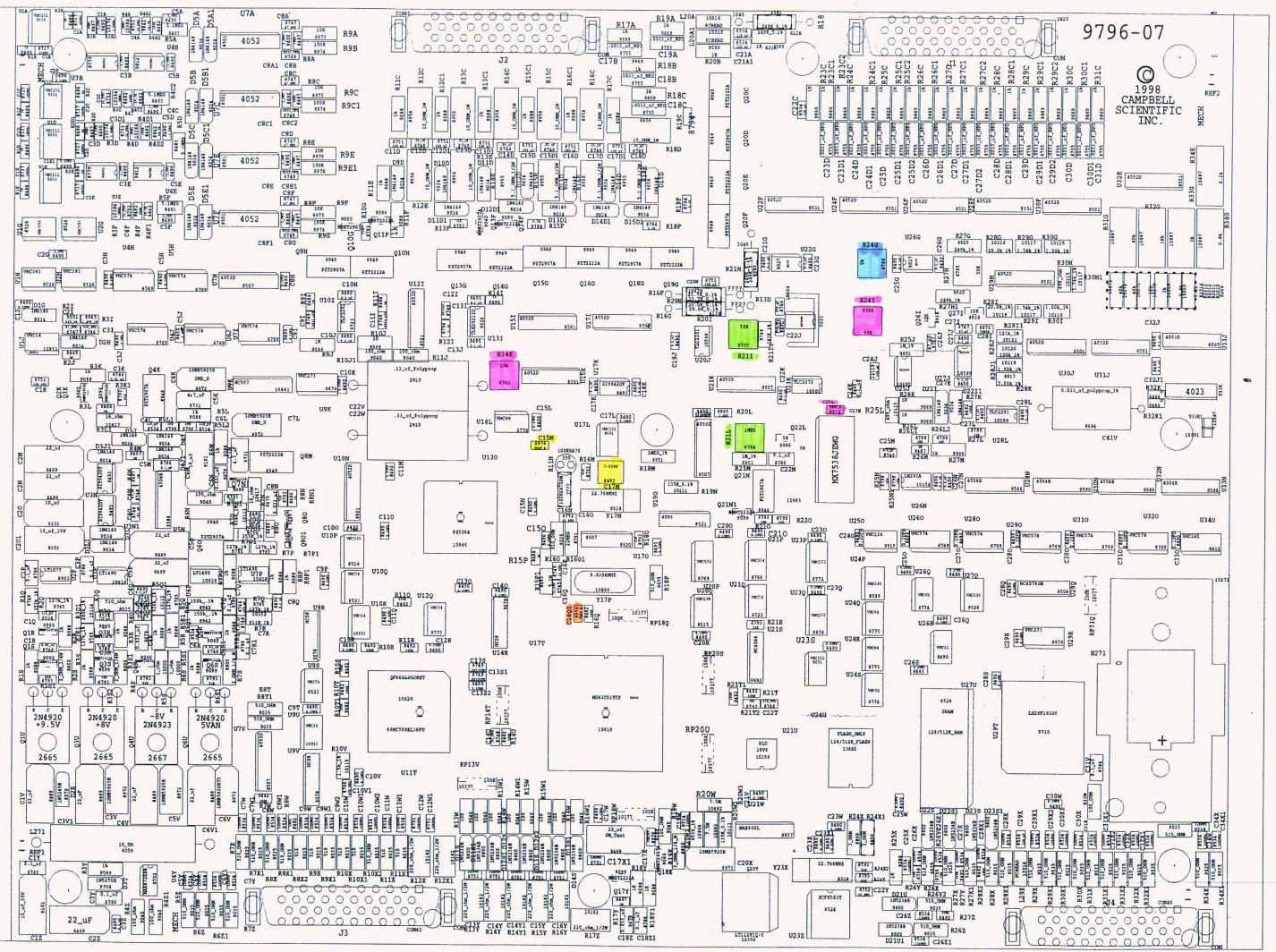
	Ex. Chan	*Del w/ex 0.01s*	*Del after/ex 0.01s*	*EX mV*
P22	*1*	*9999*	*0*	*0*

**0 (To compile program)*

A: Hook the voltmeter ground to any ground terminal that is associated with single ended or differential channels; do not use the grounds that are next to the Excitation out and CAO outs. Connect the positive lead to test point (C23L) for VDAC offset trim. Adjust pot (R24I) to 0.000 mV ± 0.05 mV on the voltmeter using a ± 200 mV or smaller input voltage range.
B: Next trim excitation offset by hooking voltmeter positive lead to the EX1 output terminal on the panel and adjusting pot (R14K) to 0.000 mV ± 0.05 mV on the voltmeter using a ± 200 mV or smaller input voltage range.

6-DAC Reference:
The voltage measurement reference is trimmed with pots (R21I), (R21L). This trimming is accomplished with an **accurate** DC voltmeter**.** With the voltmeter hooked to the EX1 terminal and the ground next to the analog input channel (not ground terminal next to EX1), trim the reference by setting the excitation in P22 output (*EX mV)* to -4000.0 mV and trim pot (R21I) for the EX1 output to read -4000.0 mV ± 0.5 mV (-3999.5 mV to 4000.5 mV). Then change P22 output (*EX mV)* to +4000 mV and trim pot (R21L) so that the EX1 output reads within +4000.0 mV ± 0.5 mV (3999.5 mV to 4000.5 mV).
Check the ± 4000 mV Excitations again and make calibrations if needed.

Calibration is completed.



NOTE:
DO NOT STUFF COMPONENTS
WITHIN DOTTED LINE.
R24X1, C16N, R20I, R20H, R21H, R22A.
R209, R2010, R2011, R2012, R2013, R2014

DESIGNED BY: JEFF_PEASE	PROJECT MANAGER: J.SWENSON	DATE OF LAST REV: 03-02-21	REV: B528
DESCRIPTION: ASY_PCS_CR23X_ANALOG_CPU			
CAMPBELL SCIENTIFIC INC		DOCUMENT NUMBER: ADR_9797-10	REV:

ORIGINAL